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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/529,626	11/23/2005	Georg Bogner	5367-163PUS	2021

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EXAMINER	
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ART UNIT	PAPER NUMBER
2892	

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11/17/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/529,626	BOGNER ET AL.	
	Examiner	Art Unit	
	AJAY K. ARORA	2892	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 August 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10,12 and 15-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) *1-10,12 and 15-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *9/29/08*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Information Disclosure Statement

1. The Information Disclosure Statement letter of 09/29/08 states that "The item of information contained in the Information Disclosure Statement was first cited in an Examination Report (copy enclosed) received from the Japanese Patent Office...." (see page 1, last paragraph). It appears that applicant is stating that a copy of the office action by Japanese Patent Office has been provided with the submission of 09/29/08. However, no such copy of office action by Japanese Patent Office has been provided and the same is also not listed in the Information Disclosure Statement. Applicant is request to clarify if applicant intends to provide a copy of the office action by the Japanese Patent Office and if so, the Information Disclosure Statement should include the same.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

4. Claims 1-7, 9, 10, 12 and 15-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Harrah (6,498,355), hereinafter Harrah, in view of Komoto (US 6,340,824), hereinafter Komoto, and further in view of Ruhnau (US 6,900,511), hereinafter Ruhnau.

The applied reference (Ruhnau) has a common inventor with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art only under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 103(a) might be overcome by: (1) a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not an invention "by another"; (2) a showing of a date of invention for the claimed subject matter of the application which corresponds to subject matter disclosed but not claimed in the reference, prior to the effective U.S. filing date of the reference under 37

CFR 1.131; or (3) an oath or declaration under 37 CFR 1.130 stating that the application and reference are currently owned by the same party and that the inventor named in the application is the prior inventor under 35 U.S.C. 104, together with a terminal disclaimer in accordance with 37 CFR 1.321(c). This rejection might also be overcome by showing that the reference is disqualified under 35 U.S.C. 103(c) as prior art in a rejection under 35 U.S.C. 103(a). See MPEP § 706.02(l)(1) and § 706.02(l)(2).

Regarding claim 1, Harrah (refer to Figure 2-4) teaches an optoelectronic component comprising:

a heat sink (6);

a carrier (30) thermally conductively connected (using 24) to the heat sink (6);

a semiconductor arrangement (28) which emits or receives electromagnetic radiation and which is arranged on the carrier (30);

external electrical connections (42/44) which are connected to the semiconductor arrangement (28), wherein the external electrical connections (42/44) are arranged in electrically insulated fashion (by dielectric layers 10 and 48) on the heat sink (6) at a distance from the carrier (30);

a basic housing (26) arranged on the heat sink (6).

However, Harrah does not teach that the basic housing comprises a "cavity" and that the semiconductor arrangement and the carrier are arranged in "a cavity defined in the basic housing" and that the said cavity "comprises an inner side which obliquely faces

the semiconductor arrangement and forms a first reflective area" for a portion of the electromagnetic radiation.

Komoto (refer to Figure 10C) teaches a cavity-type optoelectronic component, wherein a semiconductor arrangement (10 or 50) is arranged in a cavity defined in the basic housing (Col. 19, lines 35-39) and that the cavity comprises an inner side which obliquely faces (see Figure 10C) the semiconductor arrangement (10 or 50) and forms a first reflective area (Col. 19, lines 41-44) for a portion of the electromagnetic radiation It would have been obvious to one of ordinary skills in the art at the time of the invention to modify the invention of Harrah so that the semiconductor arrangement and the carrier are arranged in a cavity defined in the basic housing and that the said cavity comprises an inner side which obliquely faces the semiconductor arrangement and forms a first reflective area for a portion of the electromagnetic radiation. The ordinary artisan would have been motivated to modify Harrah for at least the purpose of providing a cavity instead of an area filled completely with resin to limit the attenuation of the LED light say by impurities in the resin, and to control light intensity in a specific direction by controlling angle of an angular/oblique reflective area.

Further, Harrah does not teach "a reflective filling compound provided between the semiconductor arrangement and the inner side of the basic housing, the reflective filling material comprising a concave curved surface extending from an inner side of the basic

housing to a top edge of the carrier and forming a second reflective area for another portion of the electromagnetic radiation".

Ruhnau (refer to Figure 1) teaches an LED package, wherein a reflective filling compound (28) provided between the semiconductor arrangement (20) and the inner side of the basic housing, the reflective filling material comprising a concave curved surface (30) extending from an inner side of the basic housing to a top edge of the carrier and forming a second reflective area for another portion of the electromagnetic radiation. It would have been obvious to one of ordinary skills in the art at the time of the invention to modify the invention of Harrah so that a reflective filling compound provided between the semiconductor arrangement and the inner side of the basic housing, the reflective filling material comprising a concave curved surface extending from an inner side of the basic housing to a top edge of the carrier and forming a second reflective area for another portion of the electromagnetic radiation. The ordinary artisan would have been motivated to modify Harrah for at least the purpose of providing control of light intensity in a specific direction (depending on the curvature of the reflective area) using a filling compound that can easily be shaped to a concave curved surface.

Regarding claim 2, Harrah (refer to Figure 2-4) teaches that the carrier (30) contains a carrier substrate and an electrically insulating layer (Col. 4, lines 51-54) arranged thereon.

Regarding claim 3, Harrah (refer to Figure 3) teaches the semiconductor arrangement (28) and the electrically insulating layer (Col. 4, lines 51-54) have an electrically conductive layer (layer to which wire bonds 48 or 50 are attached closest to semiconductor arrangement 28) arranged therebetween which is connected to one of the external electrical connections.

Regarding claim 4, Harrah (refer to Figures 2-4) teaches that the semiconductor arrangement (28) contains a semiconductor chip (Col. 2, lines 57-60).

Regarding claim 5, Harrah (refer to Figure 4) teaches that the external electrical connections (42/44) include conductor tracks (8) on a printed circuit board (52).

Regarding claim 6, Harrah (refer to Figure 4) teaches that conductor tracks (8) on different printed circuit boards (Col. 6, lines 33-37) arranged above one another form the electrical connection and are connected to one another by plated-through holes (that form vias 12) defined in the printed circuit boards.

Regarding claim 7, Harrah (refer to Figures 2-4) teaches the carrier (30) substrate has at least one material with good thermal conductivity from the group comprising Si (Col. 4, lines 51-54), diamond-coated Si, diamond, SiC, AlN and BN.

Regarding claim 9, Harrah (refer to Figures 2-4) teaches that the semiconductor arrangement (28) is attached to the carrier (30) by a metal solder (32).

Regarding claim 10, Harrah (refer to Figures 2-4) teaches that the carrier (30) is attached to the heat sink (6) by a metal solder or a thermally conductive (Col. 5, lines 1-7) adhesive (24).

Regarding claim 12, Harrah (refer to Figures 2-4) as modified above teaches that the cavity of the basic housing (26) contains only one semiconductor arrangement (28).

Regarding claim 15, Harrah teaches substantially the claimed structure but does not teach that the filling compound contains TiO_2 or an epoxy resin filled with TiO_2 particles. Komoto (refer to Figure 106) teaches an optoelectronic component, wherein the filling compound (2140a) contains TiO_2 or an epoxy resin filled with TiO_2 particles (Col. 48, lines 66-67). It would have been obvious to one of ordinary skills in the art at the time of the invention to modify the invention of Harrah so that the filling compound contains TiO_2 or an epoxy resin filled with TiO_2 particles. The ordinary artisan would have been motivated to modify Harrah for at least the purpose of providing wavelength selectivity (see Komoto, Col. 48, lines 24-34).

Regarding claim 16, Harrah (refer to Figures 2-4) teaches that the semiconductor arrangement (28) is at least partly encapsulated by a radiation-pervious encapsulation compound (26).

Regarding claim 17, Harrah (refer to Figures 2-4) teaches at least some of the external connections (42/44) are arranged between the basic housing (26) and the heat sink (6).

Regarding claims 18, 19 and 20, Harrah teaches substantially the claimed structure but does not specifically teach an electrical power consumption of the optoelectronic component id: at least 0.5 W (per claim 18), at least 1 W (per claim 19), or at least 3 W (per claim 20). It would have been an obvious matter of optimization of a recognized results driven variable by one of ordinary skills in the art at the time of the invention, to modify Harrah such that it is provided for an electrical power of at least 0.5 W, or 1 W, or 3 W respectively. Optimization of such results driven variable, for example increasing the size of heat sink, are routine in the art. The ordinary artisan would have been motivated to modify Harrah for at least the purpose of providing a high light intensity while utilizing the heatsink for effective removal of dissipated heat.

Regarding claim 21, Harrah teaches substantially the claimed structure but does not specifically teach that the optoelectronic component has a base area of no more than 1 cm^2. It would have been an obvious matter of optimization of a recognized results driven variable by one of ordinary skills in the art at the time of the invention to modify Harrah

such that the optoelectronic component has a base area of no more than 1 cm^2. The ordinary artisan would have been motivated to modify Harrah for at least the purpose of providing a high power output component with a relatively small footprint.

Regarding claim 22, Harrah teaches a component-based module, wherein the module has a plurality of optoelectronic components as claimed in claim 1 (Col. 4, lines 36-38).

5. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Harrah, Komoto and Ruhnau as applied to claims 1 and 2 above, and further in view of Jackson (US 6,800,930), hereinafter Jackson.

Regarding claim 8, Harrah (refer to Figures 2-4) teaches substantially the claimed structure including the electrically insulating layer but does not teach that the electrically insulating layer comprises SiO_2.

Jackson teaches the use of electrically insulating layer comprising SiO_2 (Col. 6, lines 55-58). It would have been obvious to one of ordinary skills in the art at the time of the invention to modify the invention of Harrah so that the electrically insulating layer comprises SiO_2. The ordinary artisan would have been motivated to modify Harrah for at least the purpose of utilizing a dielectric that has excellent adhesion to chips and substrates that often comprise silicon.

6. Claims 23 and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Harrah, Komoto and Ruhnau as applied to claim 1 above, and further in view of Stopa (US 6,318,886), hereinafter Stopa.

Regarding claim 23, Harrah teaches substantially the claimed structure including component-based module having a plurality (Col. 4, lines 36-39) of optoelectronic components as claimed in claim 1, but does not specifically disclose that "at least some of the optoelectronic components are electrically conductively connected to one another by conductor tracks".

Stopa teaches a module with plurality of optoelectronic components wherein at least some of the optoelectronic components are electrically conductively connected to one another by conductor tracks (Col. 5, lines 52-56). It would have been obvious to one of ordinary skills in the art at the time of the invention to modify the invention of Harrah so that at least some of the optoelectronic components are electrically conductively connected to one another by conductor tracks. The ordinary artisan would have been motivated to modify Harrah for at least the purpose of controlling at least some of the optoelectronic components together.

Regarding claim 24, Harrah teaches substantially the claimed structure including that the optoelectronic components are arranged in the form of a matrix (Col. 4, lines 36-39)

but does not disclose that "at least some of the optoelectronic components are connected in series".

Stopa teaches a module with plurality of optoelectronic components wherein at least some of the optoelectronic components are connected in series. It would have been obvious to one of ordinary skills in the art at the time of the invention to modify the invention of Harrah so that at least some of the optoelectronic components are connected in series. The ordinary artisan would have been motivated to modify Harrah for at least the purpose of supplying the same current to the optoelectronic components (since they are connected in series) to easily control one of the variables in the optoelectronic component light output.

Response to Arguments

7. Applicant's arguments filed 08/07/2008 have been fully considered but they are not persuasive. Whereas applicant states that a certified English translation of German priority application is enclosed with the remark (see page 2, last line and page 3, lines 1-2 of applicant's response), no such copy has actually been submitted.

8. Should applicant desire to obtain the benefit of foreign priority under 35 U.S.C. 119(a)-(d) prior to declaration of an interference, a certified English translation of the foreign application must be submitted in reply to this action. 37 CFR 41.154(b) and

41.202(e). Failure to provide a certified translation may result in no benefit being accorded for the non-English application.

Conclusion

9. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to AJAY K. ARORA whose telephone number is (571)272-8347. The examiner can normally be reached on Mon through Fri, 8am to 4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thao X. Le can be reached on (571) 272-1708. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/A. K. A./
Examiner, Art Unit 2892

/Thao X Le/
Supervisory Patent Examiner, Art Unit 2892